REMARKS

The above amendments and following remarks attend to each and every rejection and objection presented in the August 23, 2005 Office Action. Claims 1-20 remain pending, with claims 1, 13, 17 and 19 being independent.

Specification Amendment

Paragraph [0001] is amended to reference patent number 6,629,307, issued from application serial number 09/911,997, already referenced. No new matter is added. This amendment thus attends to the Examiner's objection in paragraph six of the pending office action.

Double Patenting

To overcome the double patenting rejections set forth in paragraphs 2-4 of the pending office action, we herewith file a terminal disclaimer.

Claim Rejections – 35 U.S.C. §102

Claims 1-3 and 6-20 stand rejected under 35 U.S.C. §102(e) as being anticipated by Publication No. 2003/0084418 to Regan (hereinafter "Regan"). Respectfully, we disagree.

To anticipate a claim, Regan must teach every element of the claim and "the identical invention must be shown in as complete detail as contained in the ... claim." MPEP 2131 citing Verdegaal Bros. V. Union Oil Co. of California, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) and Richardson v. Suzuki Motor Co., 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989). Regan does not teach every element of claims 1-3 and 6-20.

As way of background, the following summary may help clarify differences between Regan and the immediate application.

The immediate application teaches a system for ensuring correct connectivity between circuit designs. See at least the title and abstract of the immediate application. As shown in the example of Figure 1 and described in paragraphs [0019-21], connectivity between at least two circuit designs 32A and 32B is shown. Paragraph [0023] teaches that "mapping file 16 correlates connections between circuit designs 32." Clearly, more than one circuit design is required.

On the other hand, Regan discloses a process for modifying the design of an integrated circuit by mapping cells of an old circuit against a library of new cells and replacing at least some of the old cells with new cells to form a new circuit design. See Regan

abstract. Specifically, Regan searches a new library of cells to locate new cells that match the functionality of old cells. In paragraphs [0077-97], Regan discloses that pins of the new cells are matched with pins of the old cell, and that names of connection points are mapped because the pin names of the new cell may be different from the old cell. Thus, Regan uses pin matching when identifying a new cell to replace an old cell, and maps the connectivity of the new cell into the old circuit. However, the mapping of the new cell is within the same identical circuit. Clearly, Regan does not disclose mapping connectivity between at least two circuit designs as taught by the immediate application, nor of updating the mapping after detecting a change to the design.

More particularly, claim 1 recites a system for ensuring correct connectivity between circuit designs, including:

a) configuration files defining connections of the circuit designs;

b) at least one mapping file correlating connections between the configuration files; and

c) a processing section for updating the mapping file in response to changes of the circuit designs, and for processing the configuration files and the mapping file in generating the circuit designs.

In the system of claim 1, element a) requires configuration files defining connections of the circuit designs. As taught by paragraph [0017], symbol files 12 and geometry files 14 are collectively called "configuration files." Regan does not disclose configuration files that define connections of the circuit design nor a mapping file for correlating connections between the configuration files. The cells of Regan are not equivalent to the circuit designs of the immediate application. As noted above, Regan does not disclose connectivity between two circuit designs. Regan also does not disclose updating a mapping file in response to changes of the circuit designs, as required by step c). Further, Regan does not generate circuit designs by processing the configuration files and the mapping files. Regan only replaces once cell within a circuit design with another, equivalent cell.

For at least these reasons, Regan cannot anticipate claim 1. Reconsideration of claim 1 is respectfully requested.

Claims 2, 3 and 6-12 depend from claim 1 and benefit from like argument. These claims also have additional features that patentably distinguish over Regan. For example, claim 2 recites the mapping file initially being generated from a list of interconnectivity

signals. Regan does not disclose creation of a mapping file or of processing interconnectivity signals. Regan does not disclose initially creating a mapping file from a list of interconnectivity signals. The connections of Regan are all within a single circuit design, and are, therefore, defined by that single circuit design.

Claim 3 recites that the list comprises one or more spreadsheets. Regan does not disclose using one or more spreadsheets.

Claim 6 recites the configuration files comprise symbol files representing parts within the circuit designs. Claim 7 recites the configuration files comprise geometry files representing physical attributes of the parts. In paragraph [0003], Regan discloses "altering the placement and modifying the physical geometric data," but Regan does not disclose use of configuration, symbol or geometry files. In fact, Regan is only concerned with "modifying the design of integrated circuits." See Regan paragraph [0005]. Regan makes no reference to "files" at all, and is only concerned with libraries of components.

Claim 8 recites that the processing section is responsive to design changes of at least one of the circuit designs to automatically update the mapping file. For example, as shown in step 62 of FIG. 7 of the immediate application, connectivity changes resulting from interactive schematic editing (step 60) are detectable. Regan does not disclose detecting connectivity changes resulting from design changes of at least one of the circuit designs. Regan does not disclose a mapping file, and therefore cannot update the mapping file when connectivity changes occur. As noted above, Regan does not operate on more than one circuit design and is not concerned with connectivity between circuit designs.

Claim 9 recites that the processing section is responsive to updating of the mapping file to update at least one schematic for at least one of the circuit designs. For example, as shown in FIGs. 4, 5 and 6 and described in paragraphs [0029-30] of the immediate application, when modification of circuit design 32A is detected, mapping file 16 is updated and design 32B is automatically updated to maintain correct connectivity between circuit designs 32A and 32B. On the other hand, Regan modifies a single design of an integrated circuit and does not detect modifications nor automatically modify a second circuit design to maintain connectivity. Regan does not disclose – anywhere – updating a schematic.

Claim 10 recites that the processing section is responsive to design changes of at least one connector of the circuit designs to automatically update the mapping file. Regan is not concerned with connectors and further does not disclose updating a mapping file in response to design changes of at least one connector of the circuit design.

Claim 11 recites that the processing section is responsive to updating of the mapping file to generate at least one notification of the design changes. Since Regan does not detect design changes, Regan also does not disclose generating at least one notification of the design changes.

Claim 12 recites that the processing section generates one or more notifications indicating connectivity changes between the circuit designs. Regan does not consider connectivity between two circuit designs, and it therefore does not disclose generating one or more notifications indicating connectivity changes between the circuit designs.

For at least these reasons, Regan cannot anticipate claims 2, 3 and 6-12. Reconsideration of claims 2, 3 and 6-12 is respectfully requested.

Claim 13 recites a system for ensuring correct connectivity between circuit designs, including:

a) means for generating at least one mapping file to correlate connections between configuration files of the circuit designs;

b) means for updating the mapping file in response to a change of the circuit design; and

c) means for processing the configuration files and the mapping file in generating the circuit designs.

As argued above, Regan does not disclose connectivity between two circuit designs and therefore cannot generate a mapping file to correlate connections between configuration files of the circuit designs, as required by step a) of claim 13. Again, as argued above, Regan does not detect changes in a circuit design nor updating a mapping file is response to a change in the circuit design, as required by step b). Since Regan does not generate a mapping file, Regan cannot process the mapping file in generating the circuit designs, as required by step c).

For at least these reasons, Regan cannot anticipate claim 13. Reconsideration of claim 13 is respectfully requested.

Claims 14-16 depend from claim 13 and benefit from like argument. Theses claims also have additional features that patentably distinguish over Regan. For example, claim 14 recites the configuration files having one or both of symbol files and geometry files. As argued above, Regan does not disclose the use of symbol or geometry files; Regan is concerned only with libraries of cells. Claim 15 recites means for formulating the mapping

file from an input list. Regan does not disclose or suggest formulating the mapping file from an input list. Claim 16 recites the input list comprising a spreadsheet. As argued above, Regan does not disclose or suggest the use of a list or spreadsheet to formulate a mapping file.

For at least these reasons, Regan cannot anticipate claims 14-16. Reconsideration of claims 14-16 is respectfully requested.

Claim 17 recites a method for ensuring correct connectivity between circuit designs, comprising:

a) generating a list of connections of the circuit designs;
b) generating a mapping file from the list to correlate connections between the circuit designs; and
c) re-generating the mapping file in response to modification of at least one of the circuit designs.

As noted above, Regan is concerned only with replacing cells in a single integrated circuit design. Regan does not provide a method for ensuring connectivity between circuit designs, nor generating a list of connections of the circuit designs as required by step a) of claim 17. Since Regan does not teach connectivity between two circuit designs, Regan also does not generate a mapping file from the list of connections to correlate connections between circuit designs, as required by step b). As argued above, Regan also does not detect change to at least one of the circuit designs and therefore cannot re-generate the mapping file in response to modification of at least one of the circuit designs.

For at least these reasons, Regan cannot anticipate claim 17. Reconsideration of claim 17 is respectfully requested.

Claim 18 depends from claim 17 and benefits from like argument. Claim 18 also has additional features that patentably distinguish over Regan. For example, claim 18 recites generating at least one schematic associated with at least one of the circuit designs using information in the regenerated mapping file. Regan does not disclose – anywhere – such features.

For at least these reasons, Regan cannot anticipate claim 18. Reconsideration of claim 18 is respectfully requested.

Claim 19 recites a software product for ensuring correct connectivity between circuit designs, including:

a) generating a list of connections of the circuit designs;

b) generating a mapping file from the list to correlate connections between the circuit designs; and

c) re-generating the mapping file in response to modification of at least one of the circuit designs.

As argued above, Regan is not concerned with connectivity between circuit designs and does not generate a list of connections of the circuit designs, as required by step a) of claim 19. Regan also does not disclose generating a mapping file from the list to correlate connections between the circuit designs, as required by step b). Again, as argued above, Regan does not detect modification of at least one of the circuit designs and does not teach of generating a mapping file in response to the modification, as required by step c).

For at least these reasons, Regan cannot anticipate claim 19. Reconsideration of claim 19 is respectfully requested.

Claim 20 depends from claim 19 and benefits from like argument. Claim 20 also has other features that patentably distinguish over Regan. For example, claim 20 recites generating at least one schematic associated with at least one of the circuit designs using information in the regenerated mapping file. As argued above, Regan does not disclose – anywhere – generate a schematic.

Reconsideration of claim 1-3 and 6-20 is respectfully requested.

Claim Rejections – 35 U.S.C. §103

Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Regan in view of U.S. Patent No. 6,578,174 to Zizzo (hereinafter "Zizzo"). Respectfully we disagree.

For the purpose of the following discussion, the Examiner is respectfully reminded of the basic considerations that apply to obviousness rejections.

When applying 35 U.S.C. §103, the following tenets of patent law must be adhered to:

(A) The claimed invention must be considered as a whole;

(B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;

(C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and

(D) Reasonable expectation of success is the standard with which obviousness is determined. MPEP §2141.01, *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1134 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

In addition, it is respectfully noted that to substantiate a *prima facie* case of obviousness, the initial burden rests with the Examiner who must fulfill three requirements. More specifically:

Accordingly, to establish a *prima facie* case of obviousness, three basic criteria must be met.

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings.

Second, there must be a reasonable expectation of success.

Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The ***teaching or suggestion*** to make the claimed combination **and** the ***reasonable expectation of success*** **must *both be found in the prior art,* and not *based on applicant's disclosure***. (emphasis and formatting added) MPEP § 2143, *In re vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

Zizzo discloses "a platform which allows connection over a distributed electronic network, such as the Internet, to a plurality of end user systems to exchange and incorporate IP core design into new complex circuit designs." See Zizzo col. 4, lines 12-16. However, Zizzo does not disclose or suggest a system or method for ensuring correct connectivity ***between*** circuit designs and therefore does not overcome the shortfall of Regan, argued above.

For example, claim 4 recites a user interface for connection to one or more user stations used in generating the interconnectivity signals. Since Zizzo does not disclose interconnectivity of circuit designs, the combination of Zizzo and Regan does not disclose or suggest claim 4. Claim 5 recites a user interface for connection to one or more user stations used in inputting the changes to the circuit designs. Again, since Zizzo does not disclose interconnectivity of multiple circuit designs, the combination of Zizzo and Regan cannot disclose or suggest claim 5. In Zizzo, the connectivity between intellectual properties (IPs) is

not equivalent to interconnectivity between circuit designs as shown by FIGs. 3, 4 and 6 of the immediate application.

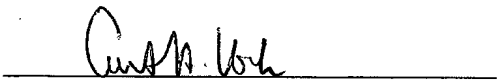
Therefore, even when combined, Regan and Zizzo cannot render independent claim 1 and dependent claims 4 and 5 obvious. Reconsideration of claims 4 and 5 is respectfully requested.

In view of the above arguments, claims 1-3 and 6-20 patentably distinguish over Regan and claims 4 and 5 are not rendered obvious by Regan in view of Zizzo.

Claims 1-20 are therefore deemed allowable. Should the Examiner disagree, we ask for the opportunity to interview.

It is believed that no fees are due in connection with this amendment. If any fee is due, please charge Deposit Account No. 08-2025.

Respectfully submitted,

By: 

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